ABSTRACT

A new method to form an integrated circuit device is achieved. The method comprises forming a dielectric layer overlying a semiconductor substrate. An intrinsic semiconductor layer is formed overlying the dielectric layer. The intrinsic semiconductor layer is patterned. A p+ region is formed in the intrinsic semiconductor layer. An n+ region is formed in the intrinsic semiconductor layer. The p+ region and said n+ region are laterally separated by an intrinsic region to thereby form a PIN diode device. A source region and a drain region are formed in the semiconductor substrate to thereby complete a MOSFET device. The PIN diode device is a gate electrode for the MOSFET device.